Reg. No. : | | | | | | | | | | | |

# G 0402

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2010

THIRD SEMESTER

ELECTRONICS COMMUNICATION ENGINEERING

EC1201 DIGITAL ELECTRONICS

(REGULATION 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State DeMorgans laws.

2. Simplify $A + \overline{A}B$ using Boolean algebra.

3. Draw a 2-input CMOS NAND gate.

4. List out the drawbacks of ECL logic family.

5. Draw a full adder circuit using two half adders and suitable gates.

6. Realize $F = \sum m(0,1,3,5,7)$ using a $4 \times 1$ multiplexer.

7. Design a Mod-4 asynchronous counter using JK flipflops.

8. Distinguish between Moore Machine and Mealy Machine.

9. What should be the size of a ROM to produce the square of a 3-bit input?

10. Define the term memory access time.

PART B — (5 × 16 = 80 marks)

11. Implement $F = \overline{(A+B)(C+D)} + A$ using NAND gates only and NOR gates only. (16)

Or

12. Reduce the expression $F = \sum m(1,5,6,12,13,14) + d(2,4)$ is SOP and POS forms. (16)

13. Explain the working of a 2-input TTL NAND gate with TOTEM POLE output. (16)

Or

14. Discuss in detail about the various specifications for a digital Integrated circuit. (16)

15. Design a 4 bit BCD to 4 bit gray code converter. (16)

Or

16. (a) Explain the working of a carry look ahead adder. (10)

(b) Design a 4 to 2 line priority encoder circuit. (6)

17. Design a 2 bit up/down counter using T flip flops. Implement using synchronous design. (16)

Or

18. Determine minimal state table using partitioning technique. (16)

| Present State | Next state X=0 | Output Z X=1 |
|---|---|---|
| S1 | S1, 1 | S1, 0 |
| S2 | S1, 1 | S6, 1 |
| S3 | S2, 0 | S5, 0 |
| S4 | S1, 0 | S7, 0 |
| S5 | S4, 1 | S3, 1 |
| S6 | S2, 0 | S5, 0 |
| S7 | S4, 1 | S3, 1 |

19. (a) Explain structure of a PROM. (8)

(b) Write short notes on RAM. (8)

Or

20. Explain in detail about static RAM cell. (16)

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